

## CLAIMS

What is claimed is:

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1 1/ A method of forming an emitter in a vertical bipolar transistor comprising:  
2 providing a substrate having a collector layer and a base layer over said  
3 collector layer;  
4 forming a patterned mask over said collector layer; and  
5 filling openings in said mask with emitter material in a damascene  
6 process.

1 2. The method in claim 1, wherein said substrate includes an insulator layer  
2 between a bottom silicon layer and a top silicon layer, said method further  
3 comprising:  
4 implanting a first impurity to form said collector layer in a lower portion  
5 of said top silicon layer adjacent said insulator layer; and  
6 implanting a second impurity to form said base layer in an upper portion  
7 of said top silicon layer.

1 3. The method in claim 2, wherein said emitter material includes said first  
2 impurity and said method further comprises annealing said vertical bipolar  
3 transistor to drive said first impurity into said base to create an emitter diffusion  
4 region in said base below each emitter.

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1 4. The method in claim 2, further comprising:  
2 patterning a second mask over said bipolar region, said mask including  
3 openings through to said base layer between adjacent ones of said emitters; and  
4 implanting additional amounts of said second impurity into said base layer  
5 through said openings.

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1 5. The method in claim 2, further comprising:  
2 forming a protective layer over said emitters; and  
3 implanting additional amounts of said first impurity into said insulator  
4 layer to provide a collector contact diffusion region.

1 6. A method of simultaneously forming complementary metal oxide  
2 semiconductor (CMOS) devices and vertical bipolar transistors on an integrated  
3 circuit chip comprising:  
4 providing a silicon over insulator (SOI) substrate having a collector layer  
5 and a base layer over said collector;

6 forming a polysilicon layer over a CMOS region of said SOI substrate;  
7 patterning a mask over said polysilicon layer and a bipolar region of said  
8 SOI substrate, said mask including openings over said bipolar region  
9 depositing an emitter material in said openings in a damascene process to  
10 form emitters;  
11 removing said mask;  
12 patterning said polysilicon layer to form gate conductors; and  
13 forming sidewall spacers adjacent said emitters and said gate conductors.

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1 7. The method in claim 6, wherein said substrate includes an insulator layer  
2 between a bottom silicon layer and a top silicon layer, said method further  
3 comprising:  
4 implanting a first impurity to form said collector layer in a lower portion  
5 of said top silicon layer adjacent said insulator layer; and  
6 implanting a second impurity to form said base layer in an upper portion  
7 of said top silicon layer.

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1 8. The method in claim 7, wherein said emitter material includes said first  
2 impurity and said method further comprises annealing said vertical bipolar  
3 transistor to drive said first impurity into said base to create an emitter diffusion  
4 region in said base below each emitter.

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1 9. The method in claim 7, further comprising:  
2 patterning a second mask over said bipolar region, said mask including  
3 second openings through to said base layer between adjacent ones of said  
4 emitters; and  
5 implanting additional amounts of said second impurity into said base layer  
6 through said openings.

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1 10. The method in claim 7, further comprising:  
2 forming a protective layer over said emitters; and  
3 implanting additional amounts of said first impurity into said insulator  
4 layer to provide a collector contact diffusion region.

1 11. The method in claim 6, further comprising, before said forming of said  
2 polysilicon, forming a gate oxide layer over said CMOS region of said SOI  
3 substrate.

1 12. A method of simultaneously forming complementary metal oxide  
2 semiconductor (CMOS) devices and vertical bipolar transistors on an integrated  
3 circuit chip comprising:  
4 providing a silicon over insulator (SOI) substrate having a collector layer

5 and a base layer over said collector;  
6 patterning a mask over a CMOS region and a bipolar region of said SOI  
7 substrate, said mask including first openings over said bipolar region;  
8 depositing an emitter material in said first openings in a first damascene  
9 process to form emitters;  
10 patterning said mask to form second openings over said CMOS region;  
11 depositing a gate conductor material in said second opening in a second  
12 damascene process to form gate conductors;  
13 removing said mask; and  
14 forming sidewall spacers adjacent said emitters and said gate conductors.

1 13. The method in claim 12, wherein said substrate includes an insulator layer  
2 between a bottom silicon layer and a top silicon layer, said method further  
3 comprising:  
4 implanting a first impurity to form said collector layer in a lower portion  
5 of said top silicon layer adjacent said insulator layer; and  
6 implanting a second impurity to form said base layer in an upper portion  
7 of said top silicon layer.

1 14. The method in claim 13, wherein said emitter material includes said first  
2 impurity and said method further comprises annealing said vertical bipolar  
3 transistor to drive said first impurity into said base to create an emitter diffusion  
4 region in said base below each emitter.

1 15. The method in claim 13, further comprising:  
2 patterning a second mask over said bipolar region, said mask including  
3 third openings through to said base layer between adjacent ones of said emitters;  
4 and  
5 implanting additional amounts of said second impurity into said base layer  
6 through said third openings.

1 16. The method in claim 13, further comprising:  
2 forming a protective layer over said emitters; and  
3 implanting additional amounts of said first impurity into said insulator  
4 layer to provide a collector contact diffusion region.

1 17. The method in claim 12, further comprising, before said forming of said  
2 polysilicon, forming a gate oxide layer over said CMOS region of said SOI  
3 substrate.

1 18. A semiconductor structure including both a CMOS transistor and a  
2 vertical bipolar transistor, comprising:  
3 a substrate having a lower semiconductor portion, an upper semiconductor  
4 portion, and an first insulator structure between said upper and lower  
5 semiconductor portions;  
6 a collector region disposed in the upper semiconductor portion, said  
7 collector region having a peak dopant concentration adjacent the first insulator  
8 structure;  
9 a plurality of base regions disposed in the upper semiconductor portion  
10 above the collector region;  
11 a plurality of emitter diffusion regions disposed in the upper  
12 semiconductor portion, each abutting a respective one of the plurality of base  
13 regions;  
14 a second insulator structure disposed on first selected portions of the upper  
15 semiconductor portion;  
16 a plurality of first electrodes disposed on the upper semiconductor portion,  
17 each of the plurality of first electrodes forming an electrical contact to a respective  
18 one of the plurality of emitter diffusion regions; and  
19 a second electrode formed on the second insulator structure, the second  
20 electrode comprising a gate electrode of the CMOS transistor.

